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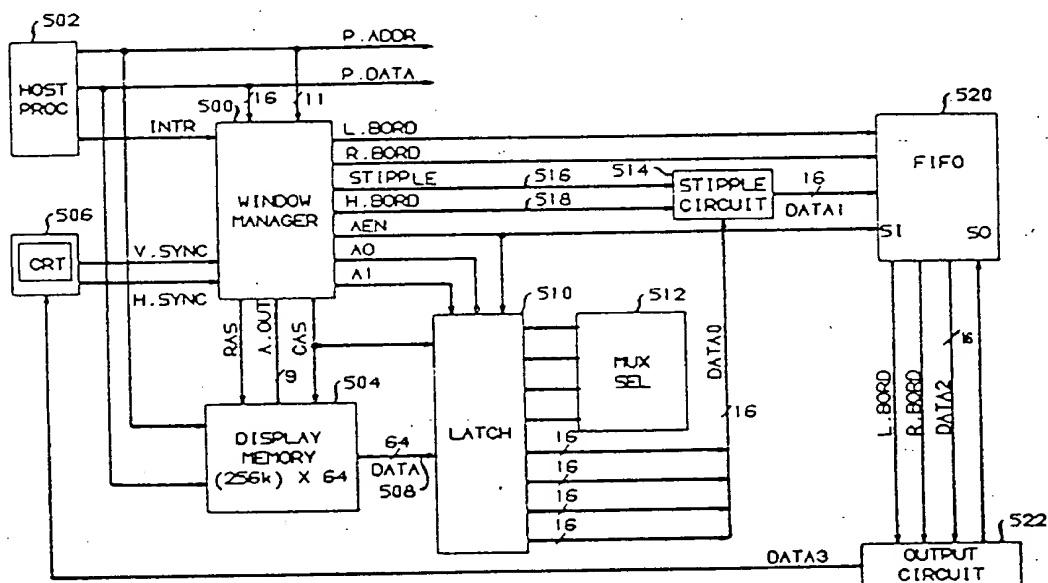
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(54) Title: BITMAPPED GRAPHICS WORKSTATION

(57) Abstract

A bitmapped graphics workstation comprising a host computer (502), window managing circuitry (500), a display memory (504), visual display device (506), and multiplexing circuitry (510, 520, 522) connecting the display memory to the display device. The window managing circuitry allows the display memory to be partitioned into plural individually contiguous bitmaps, each corresponding to a different displayed window. The window managing circuitry (500) is divided into a common control section (600) and individual window sections (602-N) corresponding to each window that may be defined. The host computer (502) writes data describing the parameters of each defined window into the individual window managing circuits. It also stores data to be displayed in the windows (including hidden data) in appropriate addresses of each of the bitmaps. As the display device (506) is refreshed, the common and the window circuits of the manager cooperate to select window "winners", i.e., the foremost window at each pixel of the screen. The appropriate contents of the bitmap corresponding to the winner at any given time is read under control of the winning window circuit sent to the display device (506) via the multiplexing circuitry.



BITMAPPED GRAPHICS WORKSTATION

Technical Field

The invention relates to the generation of
5 window borders on the displays of bitmapped graphics
workstations and the like.

Background of the Invention

"Windowing" is a feature that has recently
gained much popularity in the fields of graphics
10 workstations, personal computers, etc. The screen of a
display device, such as a workstation monitor, is
partitioned into separate rectangular areas (windows),
each of which may be assigned to view and/or control the
activities of the same or different processes being
15 carried out by an associated processor. Thus, for
example, if two windows are defined on a display screen,
a user might initiate an output printing process in one
window and then activate the second window for on-line
text processing while the background printing is
20 progressing.

Performance has been a problem with prior art
windowing techniques as applied in the field of
bitmapped graphics. Suffice it to say that the primary
reason for performance problems has been the need for
25 massive data shuffling as window data is updated. This
is caused by the manner in which data is stored for
display in prior art techniques. The prior art provides
one bitmapped display memory. The states of consecutive
bits of the memory reflect the on/off states of
30 consecutive pixels of the display screen. The bit
states are sequentially obtained from the memory and
sent to the display device as the screen of the device
is raster scanned. Thus, as scrolling is performed in

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one window, for example, large portions of the memory, corresponding to the position of the window on the display screen, must be continually updated.

By contrast, border generation for windows in the prior art bitmapped techniques is relatively simple. Since the one memory contains display data for the entire display screen, all that need be done to generate visual window borders is to set the appropriate bits in the memory to an appropriate state. The border data remains static in the memory as long as the position of the window on the screen is not changed.

Subject matter disclosed in this application and claimed in the above-mentioned co-pending application dramatically achieves an improvement in the performance of bitmapped graphics workstations. This is achieved in part by providing separate bitmaps for each defined window and by fetching screen data from appropriate places in the individual bitmaps as the display screen is refreshed. This technique, while it greatly improves performance, creates difficulty in the generation of window borders. This is because the technique, when used in conjunction with prior art border generating techniques causes a window to move on the screen as horizontal or vertical scrolling is performed in the window.

Summary of the Invention

The invention is window border generating circuitry in a bitmapped graphics workstation in which the workstation includes a host processor, a raster scanned graphics display device and means for controlling the display of data in one or more windows on the screen of the display device. An individual bitmap is provided for each window. Other memory is provided for storing parameters defining the screen boundaries of each window. Circuitry continually identifies which, if any window is presently being refreshed on the screen. At any given time, display

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data is retrieved from one of the bitmaps associated with a window presently being refreshed. The location in the bitmaps from which the display data is obtained is determined by the window boundary definitions and by the position of the raster on the screen. Circuitry is provided for detecting when the screen raster is located at a position at which a border of a window is to be displayed. Other circuitry responds to this condition by substituting for the display data from the bitmaps predefined signals for generating the screen borders.

For handling multiple windows, a depth indication, i.e., an indication of how the windows are visually stacked with respect to each other, is stored for each window. Means are provided for using the depth indications in conjunction with raster position data to determine a "winning" window if any, at each position of the screen. This determines the bitmap from which display data is obtained for each such position. Access means is provided to allow the host processor to write display data into the bitmaps.

In the preferred embodiment, windows are defined by storing addresses identifying relative horizontal screen positions of the vertical boundaries of the windows and raster line numbers identifying the horizontal boundaries of the windows. The individual bitmaps are illustratively contained in a single display memory. Display memory address generating means are provided which generates an address in an appropriate bitmap at any given time.

Border detection circuits associated with the individual windows generate border detection signals when a border area of a window with which an individual detection circuit is associated is being refreshed on the screen. A left vertical border detection signal is generated as a window is entered from the left. A right vertical border detection signal is generated as a window is exited on the right. Horizontal border

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detection signals are generated as appropriate. The border detection signals and bitmap data obtained for display are delayed to allow for border generation.

Specifically, bitmap data and the horizontal and right vertical border detection signals are delayed by a first predefined time interval. Left vertical border detection signals are delayed by a second time interval which is less than the first interval by at least the raster scan time required to scan the horizontal width of a vertical border on the screen. Output circuits respond to the delayed border detection signals to substitute border generation data signals into the delayed bitmap data. The difference in delays of the left and right vertical border detection signals allow the output circuits to generate properly and insert into the delayed bitmap the vertical border generation signals.

Brief Description of the Drawings

In the drawings,

FIG. 1 is an illustration of a display screen with two windows as they might appear in the prior art and with this invention;

FIG. 2 is an illustration of how display data is stored in a single bitmap in the prior art;

FIG. 3 illustrates how display data is stored in individual window bitmaps in the preferred embodiment of the present invention;

FIG. 4 shows an illustrative individual bitmap in the present invention with the data corresponding to individual raster lines vertically stacked so as to visually resemble a display screen;

FIG. 5 is an illustrative block diagram of the overall graphics workstation including a window manager circuit;

FIG. 6 is an illustrative block diagram of the window manager, including individual per window circuits and common circuits;

FIG 7 is a simplified view of a window backlaid with illustrative bitmap data that illustrates the effect of scrolling the window and the corresponding effects on bitmap address generation;

FIG. 8 illustrates a per window circuit that stores data defining the boundaries of a window, bitmap data for generating bitmap addresses and window depth and stipple data;

FIG. 9 illustrates a per window circuit for detecting when the associated window is being refreshed on the display device and related circuitry in a common interface circuit to a host precursor;

FIG. 10 illustrates common and per window circuitry for determining which, if any, window is being refreshed on the display device;

FIG. 11 shows an illustrative per window bitmap address generator;

FIG. 12 shows an illustrative output control circuit as part of the common circuitry and a window border detector that identifies when a window border is being refreshed on the display device;

FIG. 13 illustrates an exemplary circuit for generating window background (stipple) patterns;

FIG. 14 illustrates an exemplary output shift register circuit that generates vertical window border data and transmits this data and etched display data to the display device; and

FIG. 15 defines window area and borders in the illustrative embodiment in terms of boolean expressions of signals generated by the disclosed circuitry.

Detailed Description

FIG. 1 illustrates the face of a display screen as it might appear in an implementation of the present invention. By way of example, the screen comprises 1024 scan lines in the vertical direction with each line made up of 80 horizontal cells. Without limitation, each cell is the atomic unit of horizontal

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display in this illustrative embodiment and is composed of 16 horizontal pixels. The upper left corner of the screen is assumed to have an address of line 0 and pixel 0 (or 0,0). Similarly, the upper right corner of the screen is assumed to have a line and pixel address of 0,1264 (line 0, pixel 16*79), and so on. In the embodiment to be described, up to sixteen different work windows may be defined anywhere on the screen by a user. Different and independent work processes may typically be associated with each window. Processes associated with some windows may be idle, for example, while none, one or more processes associated with other windows are active. A user might, for example, activate an output printing process for data associated with one window and then change to another window for interactive editing while the printing is proceeding.

For illustration, the screen in FIG. 1 is assumed to be partitioned into two overlapping work windows W1 and W2. With reference to W1, the projection of its upper-left corner onto the top scan line 0 gives a left cell coordinate COORD.L for W1. Similarly, the projection of the upper-right corner onto line 0 gives a right cell coordinate address COORD.R for W1. Parameters LINE.T and LINE.B define the respective upper and lower line addresses of the window. Equivalent parameters are associated with each defined window.

FIG. 2 illustrates the manner in which window data is stored for the screen of FIG. 1 by the prior art. Individual bits of a contiguous display memory correspond one-for-one with the sequential pixels of the screen as each line is raster scanned. Thus, one contiguous segment of the memory contains the display data for a line X (shown in FIG. 1) of the screen. Part of the data in this segment corresponds to W1. A next contiguous segment contains data for line X+1, part of which corresponds to W1, and so on. It is easy to see how this leads to complexities, for example, when at

of FIG. 2, W1 and W2 begin to overlap. A scrolling of W2, for example, has to take into account the overlapping of the windows and provide for moving "hidden" data in W2 (data that is under W1) into and out of the display memory as scrolling proceeds.

By contrast, FIG. 3 illustrates the manner that display data is handled in this invention. A display memory is partitioned into a plurality of contiguous segments, each of which pertain to a potential window. Henceforth, we will refer to the entire memory as the display memory and the individual contiguous segments for each window as a bitmap. The data in each bitmap is arranged in a fashion similar to that of FIG. 2. With reference to the bitmap corresponding to W1, for example, the data to be displayed in successive lines of the window at a given time are shown in bold in FIG. 2. The arrangement of FIG. 3 reduces many of the problems of data shuffling inherent in the arrangement of FIG. 2. For example, "hidden" data is maintained in the window bitmap memory and need not be relocated as scrolling proceeds. Only that data in a window bitmap that is to be displayed is addressed at the appropriate time, as will be seen. Preferably, each bitmap is larger than that required for the full display screen. This allows any window to be any size up to the size of the screen, or to be located anywhere on the screen and also to be scrolled horizontally and vertically

The parameters ADDR.TOP, ADDR.JMP, ADDR.BASE, ADDR.BTM, W.WIDTH and B.WIDTH refer to addresses, actually relative addresses, in the individual bitmaps, rather than to screen addresses. FIG. 4 is the bitmap for W1 in which the contiguous sections pertaining to the raster lines of a screen are stacked to give the physical appearance of a screen. This presentation of the bitmap makes it easier to envision the significance of the above parameters. At any given time, ADDR.BASE

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is the bitmap address at the beginning of the window. ADDR.BTM is the last address before the end of the bitmap containing data to be displayed at any given time. ADDR.TOP is the bitmap address containing the
5 next set of line data for the window after that at ADDR.BTM. W.WIDTH is the width of the window in cells. Each cell corresponds to 16 screen pixels. B.WIDTH is the width of the display screen in cells. ADDR.JMP is the cell distance in the bitmap between the right-most
10 edge of the window and the left-most edge of the window in the next screen line (in other words, ADDR.JMP = B.WIDTH - W.WIDTH). It should be noted here that windows may or may not contain borders, as desired by a user. If a border is defined for a window the outside
15 edges of the vertical and horizontal borders correspond to the edges of the window in this illustrative embodiment. In other words a border is contained within its associated window

FIG. 7 shows a simplified 2 cell by 2 cell
20 window backlaid with characters to illustrate how scrolling is effected in the invention. The view shows characters F, G, J and K present in the windows. If the window is vertically scrolled down one cell, the host processor 502 modifies the contents of ADDR.BASE by
25 adding to it the number of raster lines assigned to one cell. This causes the window to next display the characters J, K, N and O. If then, the window is scrolled right one cell, ADDR.BASE, ADDR.TOP and ADDR.BTM must be changed. Specifically, the number of
30 pixels in a cell is added to each of these registers. This brings into view the characters K, L, O and P. The modifications to these registers to effect additional scrolling operations should now be evident. It should be noted that no bitmap data transfer is required.

35 FIG. 5 shows a block diagram of the overall system. A window manager 500 interconnects a host processor or microprocessor 502, a display memory 504, a

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display screen 506 and a number of output circuits. Processor 502 writes display data into the display memory 504 via address and data busses P.ADDR and P.DATA. Signals on lead INTR from window manager 500 to processor 502 tell the processor when it is okay to write. In addition, processor 502 writes data into internal registers of window manager 500 to control from where display data is retrieved for each window during raster scanning of display 506. Display memory 504 is illustratively a 256K by 64 bit memory (1K = 1024 bits). Data is outputted from memory 504 on bus 508 in 64 bit words. The slash in 508 indicates a multilead bus, and the number beside the slash indicates the number of leads in the bus. This notation is used throughout the disclosure. An input read address bus A.OUT extending from the window manager 500 to display memory 504, however, is only 9 bits wide, whereas 18 address bits are required to address 256K 64-bit words. Therefore, two operations are required to specify the required 18 address bits. A signal on lead RAS (row address signal) signals the first operation and a signal on lead CAS (column address signal) signals the second operation.

A 64-bit word from display memory 504 illustratively comprises data for four 16-bit contiguous cells on the display screen. The entire word is inputted into a latch 510 and the data for the individual cells metered out at appropriate times under control of a multiplexer select circuit 512. Circuit 512 is, in turn, controlled by signals on an address enable lead AEN and two address select leads A0 and A1, which identify the particular 16-bit word to be selected from the 64-bit word.

The cell data from latch 510 is routed into a stipple circuit 514 on bus DATA0. This circuit is controlled by STIPPLE signals on bus 516 and by a horizontal border detection signal H.BORD on lead 518 from the window manager 500 to add desired selective

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background textures onto the screen to individual windows and to add the horizontal portions of screen borders to the windows, if desired.

The screen data from memory 504, now modulated with stipple and horizontal border data as needed, is inputted into a first-in-first-out buffer 520 from bus DATA1 under control of signals at its shift-in (SI) input and from there outputted to an output circuit 522 under control of signals at its shift-out (SO) input. Before outputting, however, circuit 522 adds vertical window border signals to the data, as required, in accordance with the state of left and right vertical bonded signals on leads L.BORD and R.BORD. From circuit 522, display data is sent serially to the display device 506 on lead DATA3.

A more detailed block diagram of the window manager 500 is shown in FIG. 6. It comprises a common section 600 which interacts with a plurality (up to sixteen in the exemplary embodiment) of per window sections 602-1 through 602-n. A host interface circuit 614 provides the connection to a host processor 502. Each per window section may be associated with an individual window defined at any given time. Since the per window sections are identical, only the details of 602-1 are shown. A descriptor registers circuit 604-1 contains a number of registers defining the screen boundaries, border, stipple and depth of the associated window. These registers are loaded by the host processor via a host interface circuit 614 in the common section. An address generator 608-1 in the per window section uses the register data from circuit 604-1 to generate bitmap addresses for fetching screen data for the associated window. This address data is only used, however, when the respective window is actively being scanned on the screen. To determine which window, if any, is actively being scanned, a depth priority encoder 618 in the common section continuously interacts with

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window winner circuits such as 612-1 in each of the per window sections to determine a window with the highest depth at the point on the screen presently being scanned. The "in window" circuit 606-1 in each per
5 window section determines from window definition data and screen position data if the associated window is presently being scanned on the screen. At the same time, the individual window winner circuits obtain
10 respective depth information from the respective descriptor circuits, such as 604-1 and broadcasts this information to the depth priority encoder 618. Circuit 618, in turn, determines the highest depth window at any given time and returns this information to each of the window winner circuits in the per window sections.
15 Outputs from the window winner circuits 612 and the "in window" detectors 606 are examined by the respective address generators 608. If the window area being scanned on the screen is also identified as the present winner, the appropriate address generator 608 is enabled
20 and generates and passes appropriate bitmap addresses to the display memory control circuit 616 for fetching the screen update information.

A border detector 610 in each of the per window circuits detects when border areas of windows are
25 being replaced, if borders are defined, and controls the generation of special signals to create the borders on the screen. Thus, data for creating the window borders is not stored in the bitmaps. The reason for this will become apparent below.

30 These individual circuits are now described in detail. A descriptor registers circuit 604 is shown in FIG. 8. When a window is first defined, the defining data arrives on the P.DATA bus 800 from the host processor 502 and is loaded into the registers 802, 804,
35 806 and 808. These registers are respectively identified as LINE.T, LINE.B, COORD.L, and COORD.R and contain the screen parameters of the window as shown in

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FIG. 1. When a window is first defined, the host processor also determines the bitmap addresses for the parameters ADDR.TOP, ADDR.BTM, ADDR.BASE and ADDR.JMP, shown in FIGS. 3 and 4, and loads these into the
5 respective registers 810, 812, 814 and 816. Two remaining registers CNTL.DEPTH and CNTL.STIP are loaded with numbers that define the depth of a window and a background texture (stipple) for the window as displayed on the screen. These are user preferences and may be
10 changed by a user at any time by entering appropriate commands to the host processor. To load the appropriate data into the correct registers, a register address is transmitted on address bus P.ADDR with each set of register data from the host interface. A 1-out-of-N
15 translator 822 decodes the P.ADDR address into an enable signal LD1 through LD14 which identifies and enables the appropriate register for which the data is intended. Registers 810, 812, 814 and 816 contain the most significant eighteen bits of a twenty bit display memory
20 address. Therefore, two data load operations are necessary for these registers, since bus P.DATA is nine bits wide. Accordingly, two different LD signals from translator 822 are used to load each of these registers.

An "in window" detector is shown in FIG. 9
25 along with part of the host interface 614. The host interface contains three counters PIXEL.X, PIXEL.YL and PIXEL.YE. PIXEL.X keeps track of the present horizontal cell position presently being displayed on the screen. It is recalled that a cell is illustratively sixteen
30 pixels wide in the preferred embodiment. Thus, the cell clock at 900, which is being counted by PIXEL.X is really the pixel clock divided by sixteen. As the scanning of each screen line is completed, a horizontal sync signal H.SYNC at 902 from the display 506 resets
35 PIXEL.X. The signals on H.SYNC are also counted by screen line counters PIXEL.YL and PIXEL.YE. Both of these counters are reset by a vertical sync signal

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V.SYNC on lead 904 from the display 506 each time a full screen is completed. PIXEL.YE resets to zero.

PIXEL.YL, however, is arranged to reset to a negative four. The reason for having two line counters and the
5 reset value distinction has to do with window border generation, as will be seen.

The cell count is outputted on bus PX to two comparators 906 and 908. Respective secondary inputs to these comparators come from the registers COORD.L and
10 COORD.R in the descriptor registers circuit in FIG. 8. When the screen raster is at the position corresponding to COORD.L, that is entering the window on the left (see FIG. 1), comparator 906 sets a flip-flop 910. This flip-flop is reset by comparator 908 as the window is
15 exited on the right. Thus, flip-flop 910 produces a signal on its output lead XF whenever the screen raster is within the horizontal bounds of the window. This signal is delayed by one cell time by delay flip-flop 911 to generate a delayed signal on output lead XF.P.
20 This signal is used by border detector 610 to define the raster time corresponding to a vertical left or right window border and is discussed with respect to FIG. 12. Flip-flop 911 is reset at the beginning of each raster line by H.SYNC to prevent any carryover effect from the
25 immediately preceding line.

In a similar fashion as above, comparators 910, 912 and flip-flop 914 generate a signal on output lead YEF whenever the screen raster is within the vertical bounds of the window. A signal on lead YLF is
30 an image of that of YEF, but precedes YEF by four raster lines due to the reset states of PIXEL.YL and PIXEL.YE and to the action of comparators 916, 918 and flip-flop 920.

The physical meaning of the above window
35 signals can be seen easily in FIG. 15 which depicts a screen with a single window including a border. In the horizontal scanning direction, XF becomes true when the

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raster is between COORD.L and COORD.R. Note that for a window with a border, the border is inside these coordinate points. In the vertical direction, YEF is true from LINE.T (including the upper horizontal border, if any) to the bottom line of the inside of the window (i.e., not including the lower horizontal border). Conversely, YLF is true between the upper window line, not including the upper horizontal border, to the bottom line, including the bottom border. Thus, the inside of a bordered window is defined by the boolean expression (XF)(YEF)(YLF). The upper border, if any, is being scanned when the boolean expression (XF)(YEF)(YLF) is true. The bottom border, if any, is being scanned when the boolean expression (XF)(YEF)(YLF) is true. The vertical left and right borders are not defined by boolean expressions, but are handled by one-quarter cell timing delays when signal XF transitions from true to false and from false to true, as will be seen.

A window winner circuit 612 is shown on the right side of FIG. 10. The left side, separated by a vertical dotted line, is the depth priority encoder 618 in the common section of the window manager. A five lead bus 1000 extends to each of the individual window circuits. A multiple on bus 1000 to each of the other per window sections is shown at 1002. On the right side of FIG. 10, an indication of the depth of a window is brought into a comparator 1004 on bus 1006 from the descriptor registers circuit in FIG. 8. This depth indication is also received and decoded into a 1-out-of-32 signal by translator 1008, if translator 1008 is enabled, and a resulting signal is placed onto an appropriate lead of bus 1010 extending back to the depth priority encoder 618. Translator 1008 is enabled by a signal on lead 1016 generated from "in window" detector signals in FIG. 9 which, as indicated by the boolean equation $(XF)(YEF+YLF)$, occurs whenever the display raster is inside a window.

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Bus 1010 is also multiplied to the other per window circuits as indicated at multiple 1012. Encoder 618 determines the highest priority signal present on bus 1010 at any time and returns an indication of this on bus 1002 in the same format as the depth indications received from the descriptor registers circuit. Comparator 1004 in each per window circuit compares the highest priority indication from encoder 618 to its window depth and generates a signal on lead WINNER if a match is detected. This signal is also delayed by one cell time by flip-flop 1014 to produce a signal WINNER.P. WINNER.P is also used by the border generator shown in FIG. 12.

There is always a winning window in the preferred embodiment. Host processor 502 defines a default window if a user fails to do so.

Address generator 608, shown in FIG. 11, in each per window circuit uses the "in window" signals from FIG. 9 and the WINNER signal from FIG. 10 to generate bitmap addresses. Present bitmap address is maintained in a register ADDR.CUR 1100. The cell clock signal appearing on lead 1102 loads an address into register 1100 from one of the sources in the upper part of FIG. 11 at the beginning of each cell time. An output driver 1104 gates the address in register 1100 to the bitmap address leads A19' through A00' at the proper times and thence to the common portion of the window manager. Enable signals appearing on lead 1106 to driver 1104 determine when addresses are gated to these address leads. The upper boolean enabling term (WINNER)(BORDER)(YEF)(YLF), shown on lead 1106 in FIG. 11, activates driver 1104 when this window is determined to be the highest depth and a border is present. Circuitry for generating the BORDER signal is shown in FIG. 12. (YEF)(YLF) insures that the screen area being scanned is inside the border area. The signal WINNER is true only when XF is present. This

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insures that the horizontal line portion being scanned is also within the window. The bottom enabling term on lead 1106, (WINNER) (~~BORDER~~) (YEF+YLF), enables address outputting for the entire window, including the normal
5 border areas, when no border is present.

At the beginning of a screen scan, the vertical sync signal V.SYNC enables a driver 1108, which gates the base address of this window into register 1100. This prepares the starting bitmap memory address
10 when the raster first enters the window. In addition to being gated to the address bus at appropriate times, the contents of ADDR.CUR are returned on lead 1110 to one input of a fast adding circuit 1112 at the upper right corner of FIG. 11. A second input of adder 1112 is
15 attached to a positive voltage at 1114. This causes adder 1112 to increment the address from ADDR.CUR by one. This incremented address is returned and loaded into register 1100 at the beginning of each cell time while driver 1116 is enabled. The signals appearing on
20 enabling lead 1118 follow the boolean expression $(XF)(YEF)(YLF) + (XF)(YEF+YLF)$, which is true when the screen raster is inside the border and/or window area. It may be helpful to now refer to FIG. 14 which identifies the various parts of a window with
25 appropriate boolean expressions. This arrangement increments ADDR.CUR 1100 each cell time to move sequentially through the bitmap until the raster leaves the right side edge of the window on the present screen line. When the raster moves out of the window on the
30 right side of the screen, a jump in the bitmap address is made to the proper address associated with the left side of the window in the next screen line. A slow adder is used for this purpose, since time is available for address update until the raster actually arrives at
35 the next window left edge. Slow adder 1120 adds the contents of register ADDR.JMP (see FIGS. 3 and 4) to the current address. At the beginning of the next screen

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line, assuming that this line is still within the window, driver 1122 is enabled by the signal on lead 1124, (H.SYNC)((YEF)(YLF)+(YEF+YLF)), and gates the new address into ADDR.CUR.

5 Similarly, driver 1126 gates the beginning bitmap address into ADDR.CUR when it becomes necessary to loop from the bottom of the bitmap (ADDR.BOTM in FIGS. 3 and 4) to the beginning of the bitmap (ADDR.TOP). To accomplish this, comparator 1128
10 compares the contents of register ADDR.BOT in the descriptor registers circuit with ADDR.CUR and enables driver 1126 when a match occurs.

FIG. 12 shows the display memory control 616 in the common circuitry and per window circuitry that
15 cooperate to control the generation of window borders. The interface between the bitmap address generator 608 and the common circuitry is also shown. The common and per window sections are shown on the left and right of FIG. 12, respectively. First, the bitmap addressing is
20 described. Assuming that the per window circuit shown on the right of FIG. 12 is that of the winner at any given time, an appropriate address appears on the leads A19' to A00' as before described. Leads A19' through A02' appear at the input of a multiplexing circuit 1200
25 in display memory control 616. Two other inputs to multiplexer 1200 are the display memory row and column signals on leads RAS and CAS. These signals are generated by an address select circuit 1202. The
30 purpose of multiplexer 1200 and address select 1202 is to partition the address on leads A19' through A02' into two parts and to multiplex the two parts onto a nine lead address bus A.OUT. As shown in FIG. 5, A.OUT extends to the display memory 504. Address select 1202 merely toggles signals on RAS and CAS at proper times
35 based on the word clock to accomplish this purpose.

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Border detector 610, shown on the right of FIG. 12, generates signals whenever the raster coincides with a border area of a winning window. These signals cause the automatic generation of raster border signals which are modulated into the display signal stream instead of signals from display memory 504. Specifically, gates 1220, 1222 and 1224 are enabled by a signal CNTL.BORD from the descriptor register circuit in FIG. 8 if this particular window circuit has a border defined. Whenever this window circuit is the highest depth priority (WINNER true) and the raster is within the left vertical border area as defined by the boolean equation $(LF)(LF.P)$, gate 1220 activates lead L.BORD'. Similarly, gates 1222 and 1224 activate leads H.BORD' and R.BORD', respectively, when horizontal and right vertical border areas are detected for this winning circuit. L.BORD', R.BORD, and H.BORD are combined by an OR gate 1225 to generate the above-mentioned signal BORDER. NAND gate 1227 complements BORDER to form BORDER. According to the inputs to gates 1224, the R.BORD signal is generated as the window is exited on the right. To now generate the right vertical border on the screen just before the window is exited requires that the actual screen signals be generated after detecting such a window exit. This is accomplished by latch circuits described immediately below.

L.BORD' and H.BORD' are inputted to the first of three cascaded latch stages 1204, 1206 and 1208 in the display memory control. R.BORD', however, is inputted to the second latch stage 1206. Similarly, the least significant address leads A01' and A00' from address generator 608 are inputted to the first latch stage 1204 via a circuit 1210. Circuit 1210 decodes the A00' and A01' signals to generate the address enable signal AEN, which is also inputted to the first delay stage 1204. The corresponding output signals from the third stage 1208, A00, A01, AEN, L.BORD, H.BORD and

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R.BORD are the signals actually used for controlling the screen image. A given cell clock signal at latch 1204 gates in the states of its inputs. Two cell clock signals later, these states appear at the output of latch 1208. The one cell difference in delay between R.BORD and L.BORD created by latches 1206 and 1204 is used by the output current 522 to create right edge window borders, as will be seen.

An AND gate 1219 in the per window circuitry is enabled when the associated window is the winning window. This causes stipple pattern select signals from the descriptor registers to also be gated to the input of first latch 1204. The corresponding delayed output signals appear at the output STIPPLE of latch 1208 in synchronizing with the above-described signals for controlling the actual display of data.

Horizontal border generation on the screen, as well as background window stipple patterns are generated by the stipple circuit 514. The details of circuit 514 are shown in FIG. 13.

A stipple pattern selected circuit 1300 receives the STIPPLE signals to select the pattern for the associated window. A counter 1302 is used to keep track of the pixel spacing between the stipples (e.g., data). Counter 1302 is reset at the beginning of a screen by V.SYNC which is applied to the counter via OR gate 1304. H.SYNC increments counter 1302. Selector 1300 reads the counter outputs to detect when a stipple should be inserted into the display data stream (or determined by the selected stipple pattern). When this occurs, selector 1300 applies a data signal to lead 1306 and a signal to lead 1308 to reset counter 1302. The signal on lead 1306 is injected into the display data stream on DATA0 by an EXCLUSIVE OR gate 1310. The output of gate 1310 extends to a NAND gate 1310. The output of gate 1310 extends to a NAND gate 1312 which outputs the stream to bus DATA1. Bus

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DATAL extends to FIFO 520 where the data signals are temporarily stored. Signals for creating a horizontal border on the display device are injected at gate 1312 whenever a H.BORD signal appears on lead 1314.

5 The output control 522 in FIG. 14 performs the final operations to generate the vertical window borders. Cell data from FIFO 520 appears on incoming bus 1400 in sixteen bit parallel format. The eight most significant of these bits are inputted to a shift
10 register 1402 and the eight least significant bits are put into another shift register 1404, both under control of a shift out signal S0, described below. When no border considerations are present, signals on leads LSR and MSR cause the data to be shifted out serially from
15 SR 1404 to the display device 506 via OR gate 1406 and simultaneously from SR 1402 to SR 1404.

 Signals on leads LSR and MSR are generated as follows. Gate 1408 is activated when neither L.BORD or R.BORD is present. An output signal of gate 1408
20 activates a tick circuit 1410. Circuit 1410, in turn, then outputs a stream of sixteen pulses to OR gates 1412 and 1414 in synchronism with pixel clock pulses to shift out one cell of data from SRs 1402 and 1404. At the end of the sixteen pulse stream, tick circuit applies a
25 signal to OR gate 1416 to generate the S0 signal. This signal is returned to FIFO 520 to gate out another cell of data. Simultaneously, it gates that data into SRs 1402 and 1404. When a left-edge border is detected L.BORD activates gate 1418, which, in turn, activates
30 tick circuit 1420. Four pulses are applied to OR gate 1422 as a result. The resulting four signals on lead LBSR shift out four fixed signals from a SR 1424 to inject a four pixel wide portion of a vertical border. At the end of this interval, tick circuit 1420 activates
35 tick circuit 1426, which pulses gates 1412 and 1414 to shift out another cell of data from SRs 1402 and 1404. When this is accomplished, circuit 1426 pulses OR

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gate 1416 to generate SO. Gate 1428 is activated when a right-edge border is detected. In response, tick circuit 1430 generates 12 tick pulses. The first eight of these cause eight data bits to be outputted from the least significant SR 1404. Simultaneously, twelve border signals are shifted into SR 1404 by the tick signals applied to OR gate 1432. The first four of these border signals will eventually be outputted from SR 1404 to the data stream. The remaining will be replaced by new cell data from FIFO 520, as described.

It is to be understood that the above-described arrangements are merely illustrative of the many possible specific embodiments which can be devised to represent application of the principles of the invention. Numerous and varied other arrangements can be devised in accordance with these principles by those skilled in the art without departing from the spirit and scope of the invention.

CLAIMS

1. A bitmapped graphics workstation
comprising

5 a host processor, a visual output display
device having a raster scanned display screen, and means
for defining a plurality of independent window areas on
the screen and for controlling the display of data in
each of the windows, said means for defining and
controlling further comprising
10 a plurality of bitmap storage areas each
having contiguous storage words addressable by the host
processor for storing display data associated with a
different said window,
means for storing definitions of window
15 boundaries on the screen,
means responsive to the window defining means
for identifying when the screen raster is refreshing an
area of the screen associated with a defined window,
means activated by the identifying means for
20 retrieving display data from one of the bitmap storage
areas associated with the window at locations thereof
associated with the screen position of the raster, and
means for transmitting the retrieved display
data to the display device in synchronism with the
25 raster.

2. The invention of claim 1 in which the
defining and controlling means further comprises
means for storing an individual depth
indication for each defined window identifying a
30 conceptual layer on the screen for the window,
means for identifying from the stored depth
indications a winning window, if any, having the highest
depth priority at every display entity on the screen,
and
35 means responsive to the winner identifying
means for retrieving display data for the screen display
entity from the bitmap associated with the winning

window.

3. The invention of claim 2 in which the means for retrieving display data from the bitmaps further comprises

5 means responsive to the window defining means for generating an address in the winning window bitmap associated with the screen display entity.

4. The invention of claim 3 further comprising

10 first access means for allowing the host processor to write display data into the bitmaps.

5. The invention of claim 4 further comprising

15 second access means for allowing the host processor to write window defining data into the window boundary storing means.

6. The invention of claim 5 further comprising

20 means for modulating into the display data sent to the display device signals for creating a background stipple pattern for the windows.

7. The invention of claim 6 further comprising

25 means for specifying individual stipple patterns for each window.

8. The invention of claim 7 wherein the stipple specifying means further comprises

means for storing individual stipple pattern indications for each window.

30 9. The invention of claim 8 further comprising

third access means for allowing the host processor to write data into the stipple pattern storing means.

35 10. The invention of claim 1 wherein the means for in window detection further comprise

means for storing data representing screen coordinate positions which define the position of the associated window on the screen,

first counter means for identifying the
5 horizontal position of the raster on the screen,

second counter means for identifying the vertical position of the raster on the screen, and

means for comparing the window coordinate data with the contents of the first and second counters, and

10 means responsive to the comparing means for generating in window signals.

11. The invention of claim 10 wherein a said bitmap address identifies a word of display data of a prescribed width and wherein the first counter means
15 identifies a horizontal position on a scan line of the display device that is an integer subdivision of the prescribed width of a said word.

12. The invention of claim 1 wherein the bitmap address generating means further comprises

20 first means for storing an address of a bitmap word associated with the beginning of the associated window on the screen when scanned from top-to-bottom and left-to-right,

second means for storing a bitmap address
25 offset value representing the bitmap address distance between the right vertical edge of the associated window in one scan line on the screen and the beginning of the left vertical edge of the window in the next consecutive scan line of the screen,

30 third means for storing a bitmap address corresponding to the last word in the bitmap containing data associated with the window, and

fourth means for storing a bitmap address
35 identifying the first word in the bitmap associated with the window,

fifth means for storing a present bitmap
address,

means for incrementing the contents of the
last-mentioned storing means in synchronism with

5 movement of the raster,

means for gating the contents of the first
storing means into the fifth storing means when the
window is initially entered on each screen refresh,

means for adding the contents of the second
10 storing means to the contents of the fifth storing means
when the window is exited at the right vertical edge,
and

means for gating the contents of the fourth
storing means into the fifth storing means when the
15 present bitmap address equals the contents of the third
storing means.

13. A bitmapped graphics workstation
comprising

a host processor,
20 a visual output display device having a raster
scanned display screen, and

means for defining a plurality of independent
display window on the screen and for controlling the
display of data in each of the windows, said means for
25 defining and controlling further comprising

a common circuit connected to a plurality of
individual window circuits,

the common circuit including a plurality of
bitmaps individually associated with the window
30 circuits,

and the window circuits each including
means for storing prescribed types of data
defining a window

means responsive to the window defining data
35 and to screen synchronization signals for detecting when
the screen raster is in the window on the screen, and

means responsive to the window defining data to the "in window" detecting means and to the synchronization signals for generating addresses in the bitmap associated with the window,

5 and wherein the common circuit further comprises

means for retrieving screen display data from the bitmaps responsive to the addresses from the individual window circuits, and

10 means for transmitting the retrieved data serially to the display device in synchronization with the screen raster.

14. The invention of claim 13 in which each window circuit further comprises

15 means for storing an individual depth indication identifying a conceptual layer on the screen for its associated window, and

means in the "in window" detecting means for transmitting the depth indication to the common circuit when the screen raster is inside the screen window, wherein the common circuit further comprises

means for identifying from the depth indications received from the window circuits a winning window, if any, having the highest depth priority at every display entity on the screen, and

25 means for transmitting an indication of the winning window to the window circuits.

15. The invention of claim 14 wherein the "in window" detecting means further comprises

30 means for determining from the winning window indication whether or not this window circuit is associated with the winning window.

16. The invention of claim 15 in which the bitmap address generating means further comprises

35 means responsive to a signal from the determining means for activating the bitmap address generation means.

17. The invention of claim 16 further comprising

first access means for allowing the host processor to write display data into the bitmaps.

5 18. The invention of claim 17 further comprising

second access means for allowing the host processor to write window defining data into the window defining storing means.

10 19. The invention of claim 18 further comprising

means for modulating into the display data sent to the display device signals for creating a background stipple pattern for the windows.

15 20. The invention of claim 19 further comprising

means for specifying individual stipple patterns for each window.

20 21. The invention of claim 20 wherein the stipple specifying means further comprises

means for storing individual stipple pattern indications for each window.

22. The invention of claim 21 further comprising

25 third access means for allowing the host processor to write data into the stipple pattern storing means.

23. The invention of claim 13 wherein the means for "in window" detection further comprise

30 means for storing data representing screen coordinate positions which define the position of the associated window on the screen,

first counter means for identifying the horizontal position of the raster on the screen,

35 second counter means for identifying the vertical position of the raster on the screen, and

means for comparing the window coordinate data with the contents of the first and second counters, and means responsive to the comparing means for generating "in window" signals.

5 24. The invention of claim 13 wherein the bitmap address generating means further comprises first means for storing an address of a bitmap word associated with the beginning of the associated window on the screen when scanned from top-to-bottom and
10 left-to-right,

second means for storing a bitmap address offset value representing the bitmap address distance between the right vertical edge of the associated window in one scan line on the screen and the beginning of the
15 left vertical edge of the window in the next consecutive scan line of the screen,

third means for storing a bitmap address corresponding to the last word in the bitmap containing data associated with the window, and

20 fourth means for storing a bitmap address identifying the first word in the bitmap associated with the window, fifth means for storing a present bitmap address,

means for incrementing the contents of the
25 last-mentioned storing means in synchronism with movement of the raster.

means for gating the contents of the first storing means into the fifth storing means when the window is initially entered on each screen refresh,

30 means for adding the contents of the second storing means to the contents of the fifth storing means when the window is exited at the right vertical edge, and

means for gating the contents of the fourth
35 storing means into the fifth storing means when the present bitmap address equals the contents of the third storing means.

25. One or more integrated semiconductor circuit chips for interfacing with a host processor, and a raster scanned visual output display device having a raster scanned display screen, said one or more chips comprising

means for defining a plurality of independent window areas on the screen and for controlling the display of data in each of the windows, said means for defining and controlling further comprising

a plurality of bitmap storage areas each having contiguous storage words addressable by the host processor for storing display data associated with a different said window,

means for storing definitions of window boundaries on the screen,

means responsive to the window defining means for identifying when the screen raster is refreshing an area of the screen associated with a defined window,

means activated by the identifying means for retrieving display data from one of the bitmap storage areas associated with the window at locations thereof associated with the screen position of the raster, and

means for transmitting the retrieved display data to the display device in synchronism with the raster.

26. The invention of claim 25 in which the defining and controlling means further comprises

means for storing an individual depth indication for each defined window identifying a conceptual layer on the screen for the window,

means for identifying from the stored depth indications a winning window, if any, having the highest depth priority at every display entity on the screen,

and

means responsive to the winner identifying means for retrieving display data for the screen display entity from the bitmap associated with the winning window.

5 27. The invention of claim 26 in which the means for retrieving display data from the bitmaps further comprises

 means responsive to the window defining means for generating an address in the winning window bitmap
10 associated with the screen display entity.

 28. The invention of claim 27 further comprising

 first access means for allowing the host processor to write display data into the bitmaps.

15 29. The invention of claim 28 further comprising

 second access means for allowing the host processor to write window defining data into the window boundary storing means.

20 30. The invention of claim 29 further comprising

 means for modulating into the display data sent to the display device signals for creating a background stipple pattern for the windows.

25 31. The invention of claim 30 further comprising

 means for specifying individual stipple patterns for each window.

30 32. The invention of claim 31 wherein the stipple specifying means further comprises

 means for storing individual stipple pattern indications for each window.

 33. The invention of claim 32 further comprising

35 third access means for allowing the host processor to write data into the stipple pattern storing means.

34. The invention of claim 25 wherein the means for "in window" detection further comprise

means for storing data representing screen coordinate positions which define the position of the
5 associated window on the screen,

first counter means for identifying the horizontal position of the raster on the screen,

second counter means for identifying the vertical position of the raster on the screen, and

10 means for comparing the window coordinate data with the contents of the first and second counters, and
means responsive to the comparing means for generating "in window" signals.

35. The invention of claim 25 wherein the
15 bitmap address generating means further comprises

first means for storing an address of a bitmap word associated with the beginning of the associated window on the screen when scanned from top-to-bottom and left-to-right,

20 second means for storing a bitmap address offset value representing the bitmap address distance between the right vertical edge of the associated window in one scan line on the screen and the beginning of the left vertical edge of the window in the next consecutive
25 scan line of the screen,

third means for storing a bitmap address corresponding to the last word in the bitmap containing data associated with the window, and

fourth means for storing a bitmap address
30 identifying the first word in the bitmap associated with the window,

fifth means for storing a present bitmap address,

means for incrementing the contents of the
35 last-mentioned storing means in synchronism with movement of the raster,.

means for gating the contents of the first storing means into the fifth storing means when the window is initially entered on each screen refresh,

means for adding the contents of the second storing means to the contents of the fifth storing means when the window is exited at the right vertical edge, and

means for gating the contents of the fourth storing means into the fifth storing means when the present bitmap address equals the contents of the third storing means.

36. One or more integrated semiconductor circuit chips for interfacing with

a host processor, and
a raster scanned visual output display device having a raster scanned display screen, said one or more chips comprising

means for defining a plurality of independent display windows on the screen and for controlling the display of data in each of the windows, said means for defining and controlling further comprising

a common circuit connected to a plurality of individual window circuits,

the common circuit including a plurality of bitmaps individually associated with the window circuits,

and the window circuits each including

means for storing prescribed types of data defining a window

means responsive to the window defining data and to screen synchronization signals for detecting when the screen raster is in the window on the screen, and

means responsive to the window defining data to the "in window" detecting means and to the synchronization signals for generating addresses in the bitmap associated with the window,

and wherein the common circuit further
comprises

means for retrieving screen display data from
the bitmaps responsive to the addresses from the
5 individual window circuits, and

means for transmitting the retrieved data
serially to the display device in synchronization with
the screen raster.

37. The invention of claim 36 in which each
10 window circuit further comprises

means for storing an individual depth
indication identifying a conceptual layer on the screen
for its associated window, and

means in the "in window" detecting means for
15 transmitting the depth indication to the common circuit
when the screen raster is inside the screen window,
wherein the common circuit further comprises

means for identifying from the depth
indications received from the window circuits a winning
20 window, if any, having the highest depth priority at
every display entity on the screen, and

means for transmitting an indication of the
winning window to the window circuits.

38. The invention of claim 37 wherein the "in
25 window" detecting means further comprises

means for determining from the winning window
indication whether or not this window circuit is
associated with the winning window.

39. The invention of claim 38 in which the
30 bitmap address generating means further comprises

means responsive to a signal from the
determining means for activating the bitmap address
generation means.

40. The invention of claim 39 further
35 comprising

first access means for allowing the host processor to write display data into the bitmaps.

41. The invention of claim 40 further comprising

5 second access means for allowing the host processor to write window defining data into the window defining storing means.

42. The invention of claim 41 further comprising

10 means for modulating into the display data sent to the display device signals for creating a background stipple pattern for the windows.

43. The invention of claim 42 further comprising

15 means for specifying individual stipple patterns for each window.

44. The invention of claim 43 wherein the stipple specifying means further comprises

20 means for storing individual stipple pattern indications for each window.

45. The invention of claim 44 further comprising

25 third access means for allowing the host processor to write data into the stipple pattern storing means.

46. The invention of claim 36 wherein the means for "in window" detection further comprise

30 means for storing data representing screen coordinate positions which define the position of the associated window on the screen,

first counter means for identifying the horizontal position of the raster on the screen,

second counter means for identifying the vertical position of the raster on the screen, and

35 means for comparing the window coordinate data with the contents of the first and second counters, and

means responsive to the comparing means for generating "in window" signals.

47. The invention of claim 36 wherein the bitmap address generating means further comprises

5 first means for storing an address of a bitmap word associated with the beginning of the associated window on the screen when scanned from top-to-bottom and left-to-right,

second means for storing a bitmap address
10 offset value representing the bitmap address distance between the right vertical edge of the associated window in one scan line on the screen and the beginning of the left vertical edge of the window in the next consecutive scan line of the screen,

15 third means for storing a bitmap address corresponding to the last word in the bitmap containing data associated with the window, and

fourth means for storing a bitmap address identifying the first word in the bitmap associated with
20 the window,

fifth means for storing a present bitmap address,

means for incrementing the contents of the last-mentioned storing means in synchronism with
25 novement of the raster,

means for gating the contents of the first storing means into the fifth storing means when the window is initially entered on each screen refresh,

means for adding the contents of the second
30 storing means to the contents of the fifth storing means when the window is exited at the right vertical edge, and

means for gating the contents of the fourth storing means into the fifth storing means when the
35 present bitmap address equals the contents of the third storing means.

FIG. 1

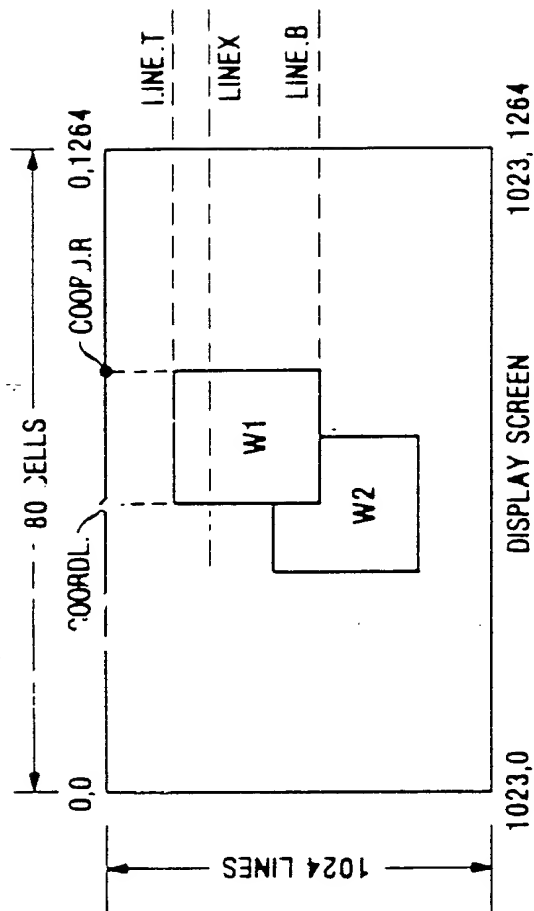
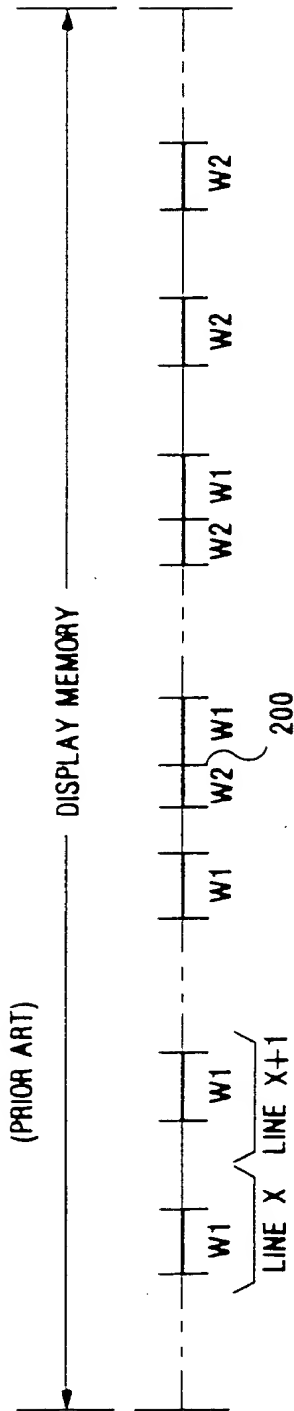


FIG. 2
(PRIOR ART)



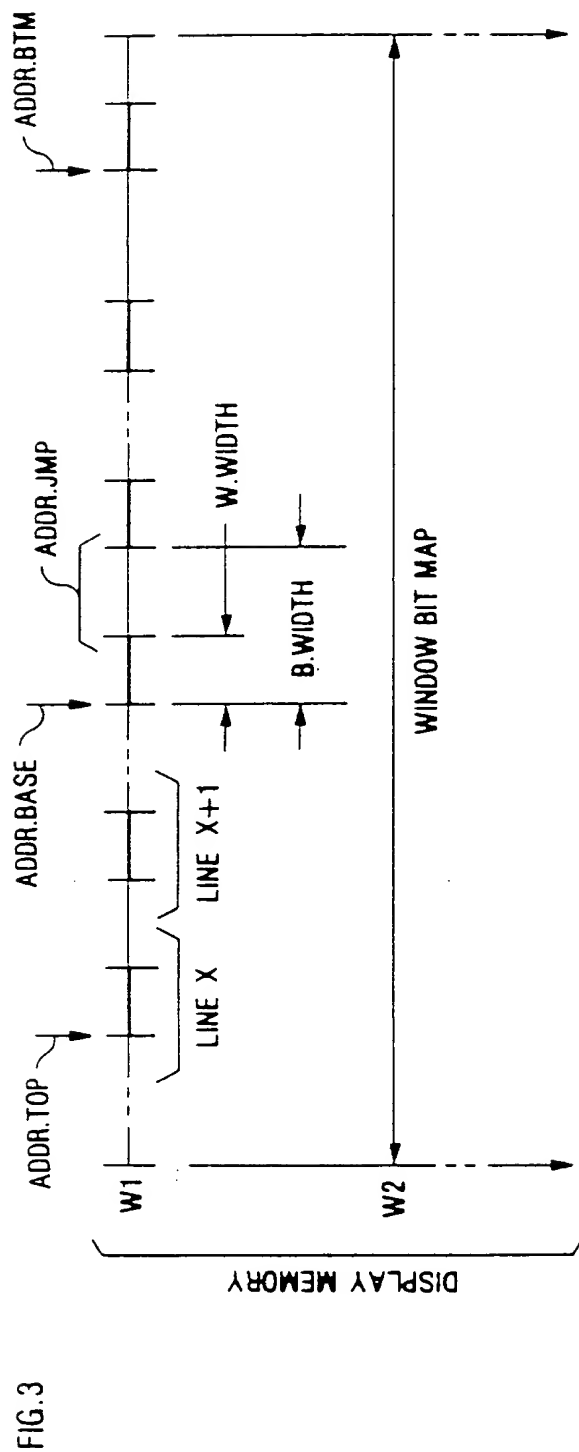
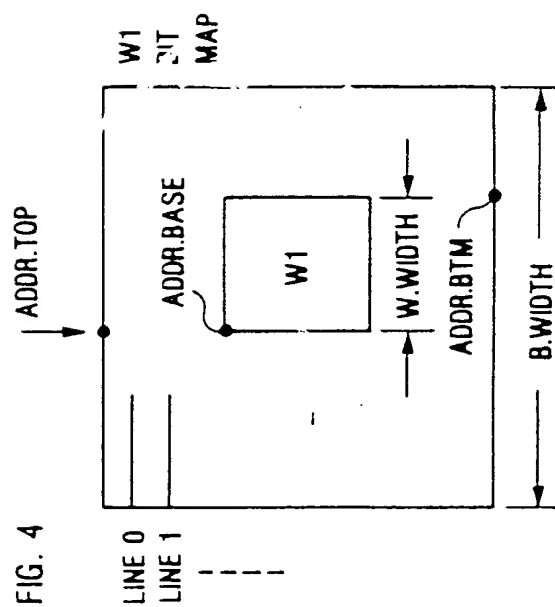


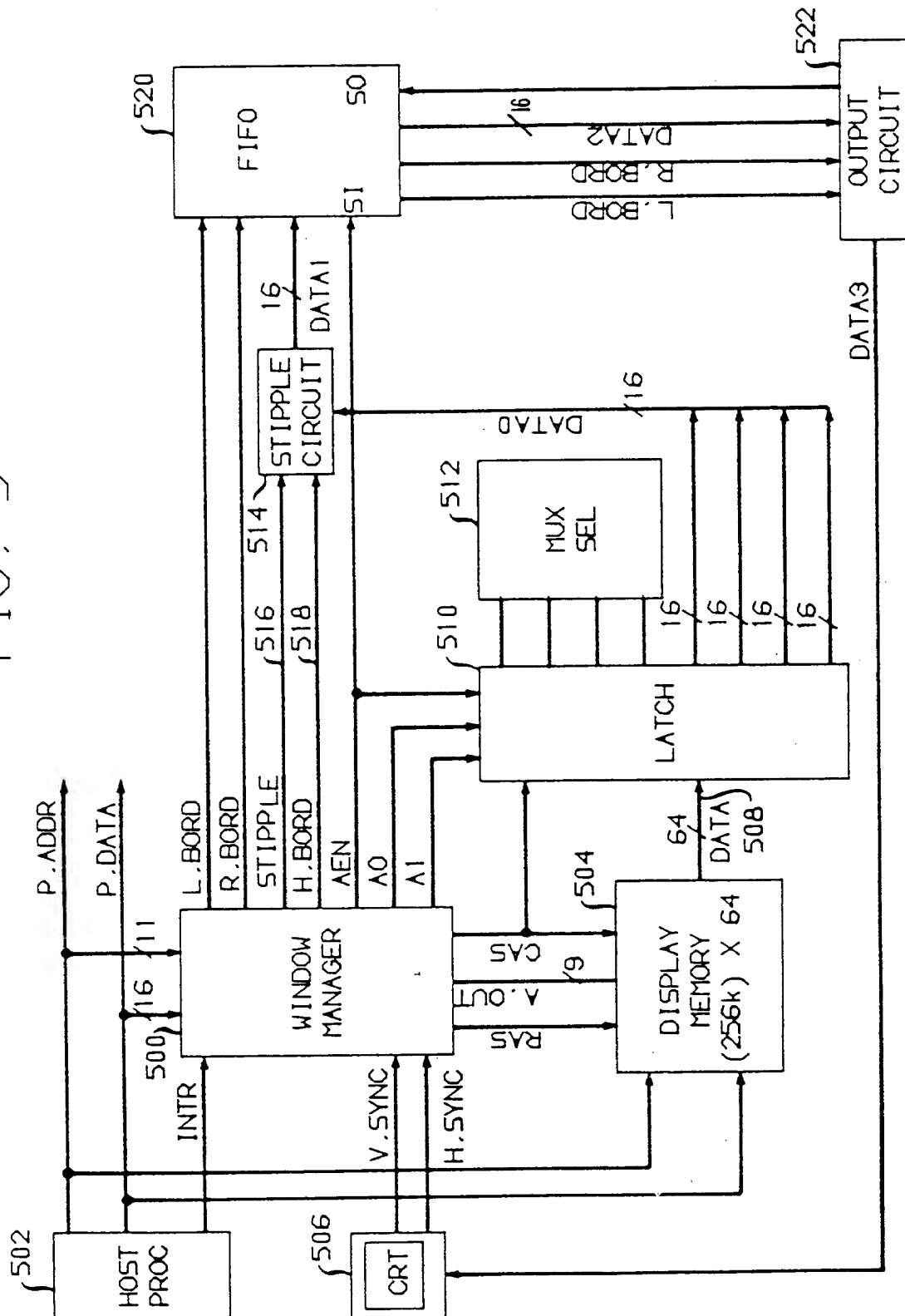
FIG. 7

		D	H	L	P
		C	G	K	O
		B	F	J	N
		A	E	I	M



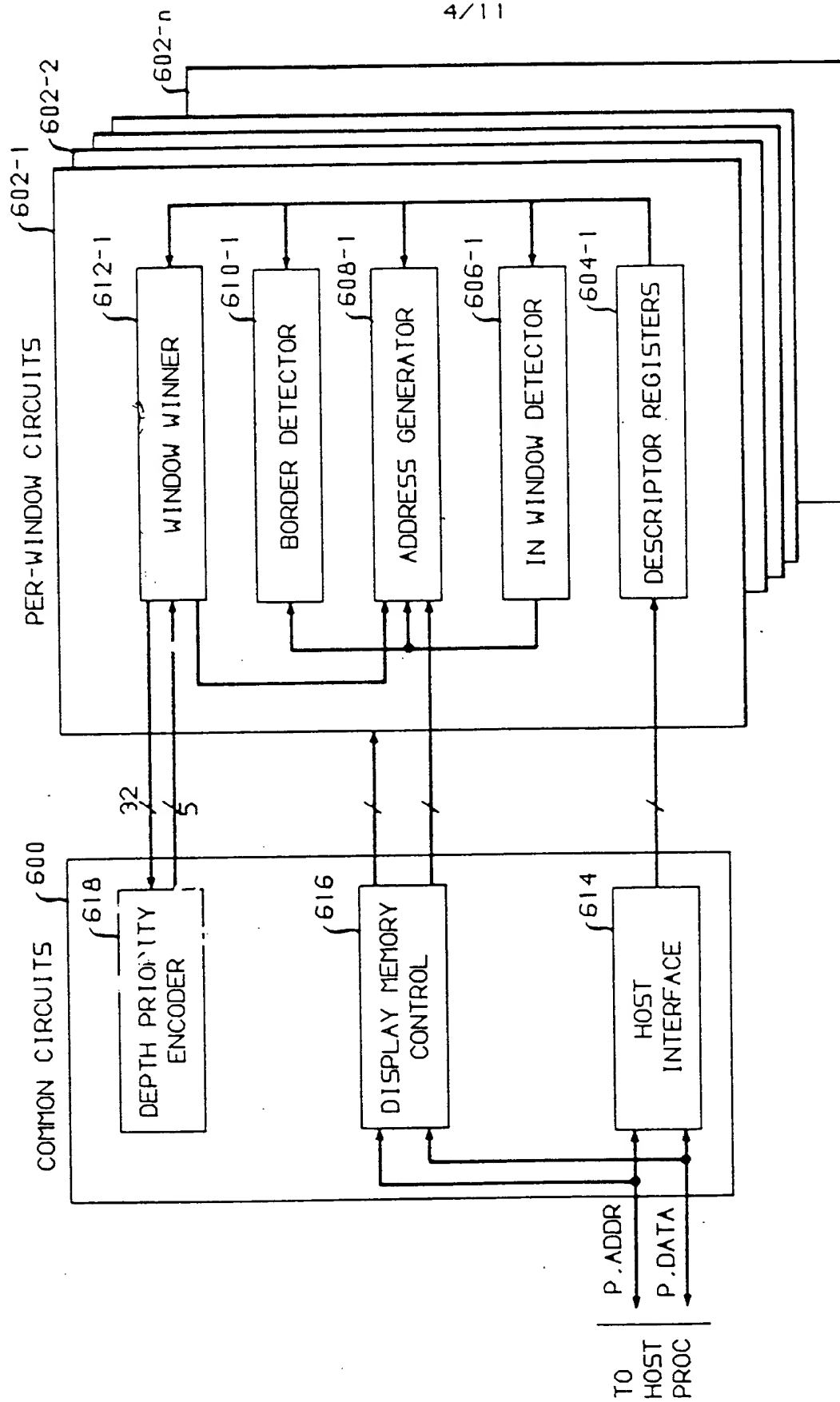
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FIG. 5



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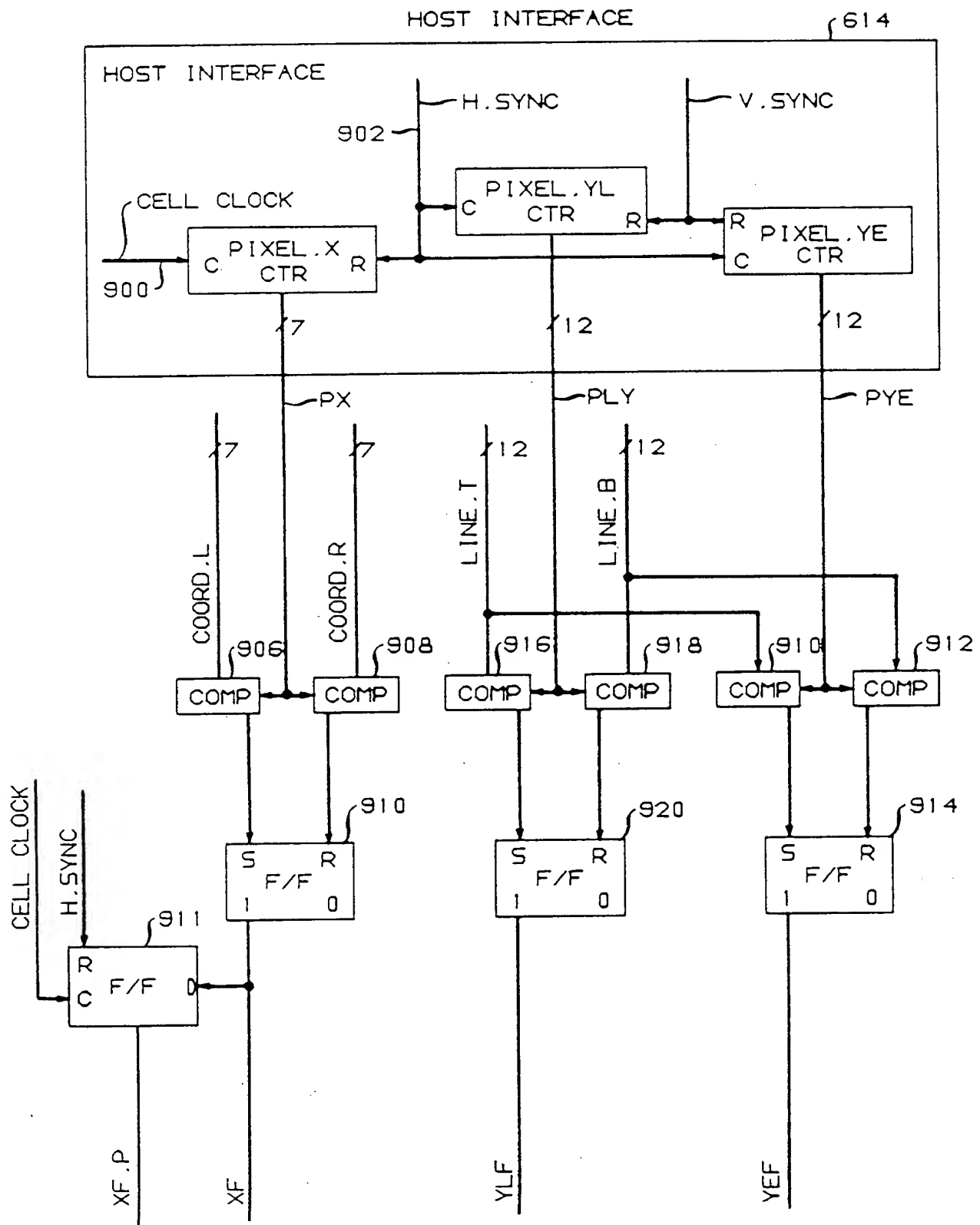
FIG. 6



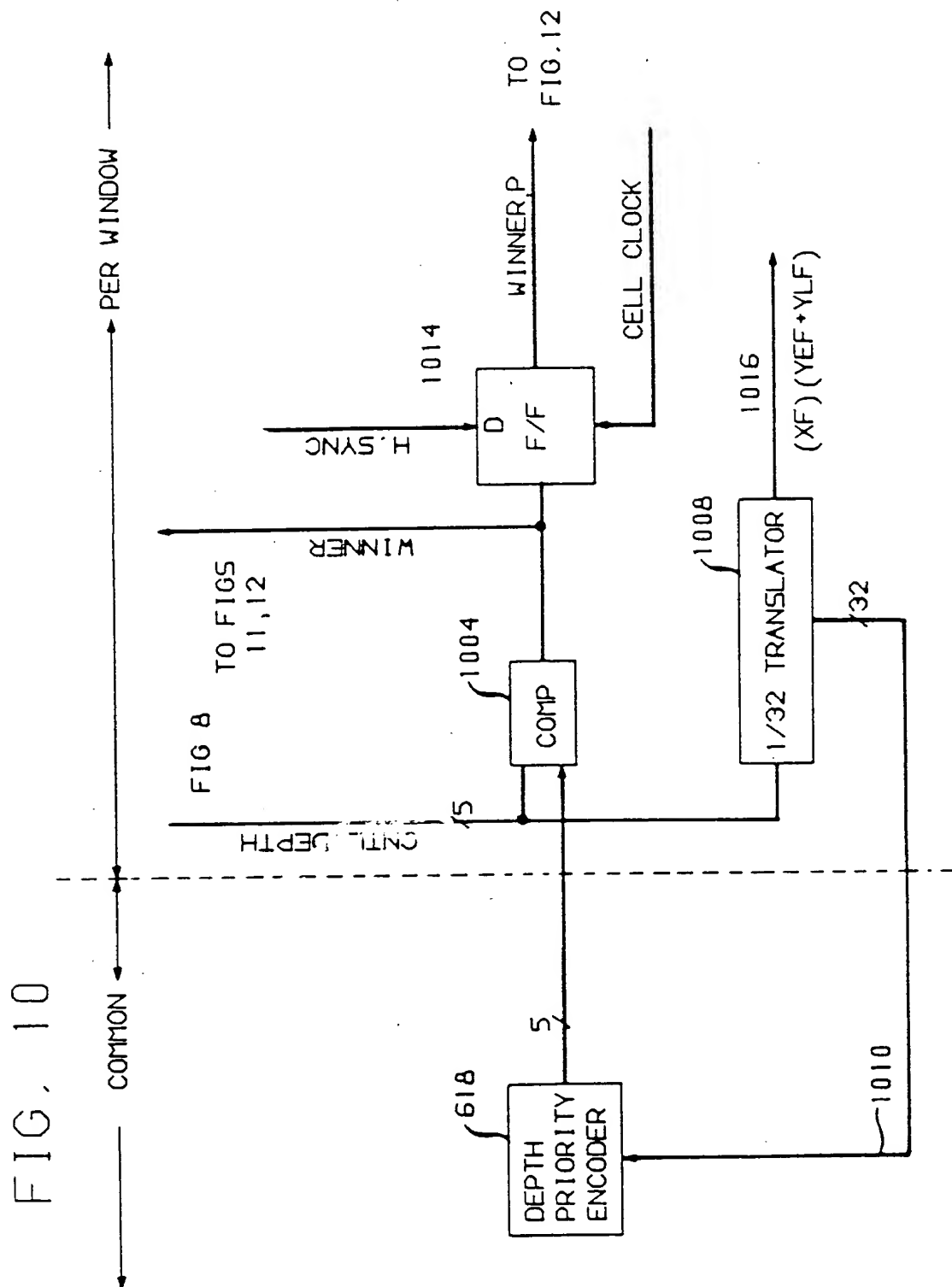
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FIG. 9

'IN WINDOW' DETECTOR

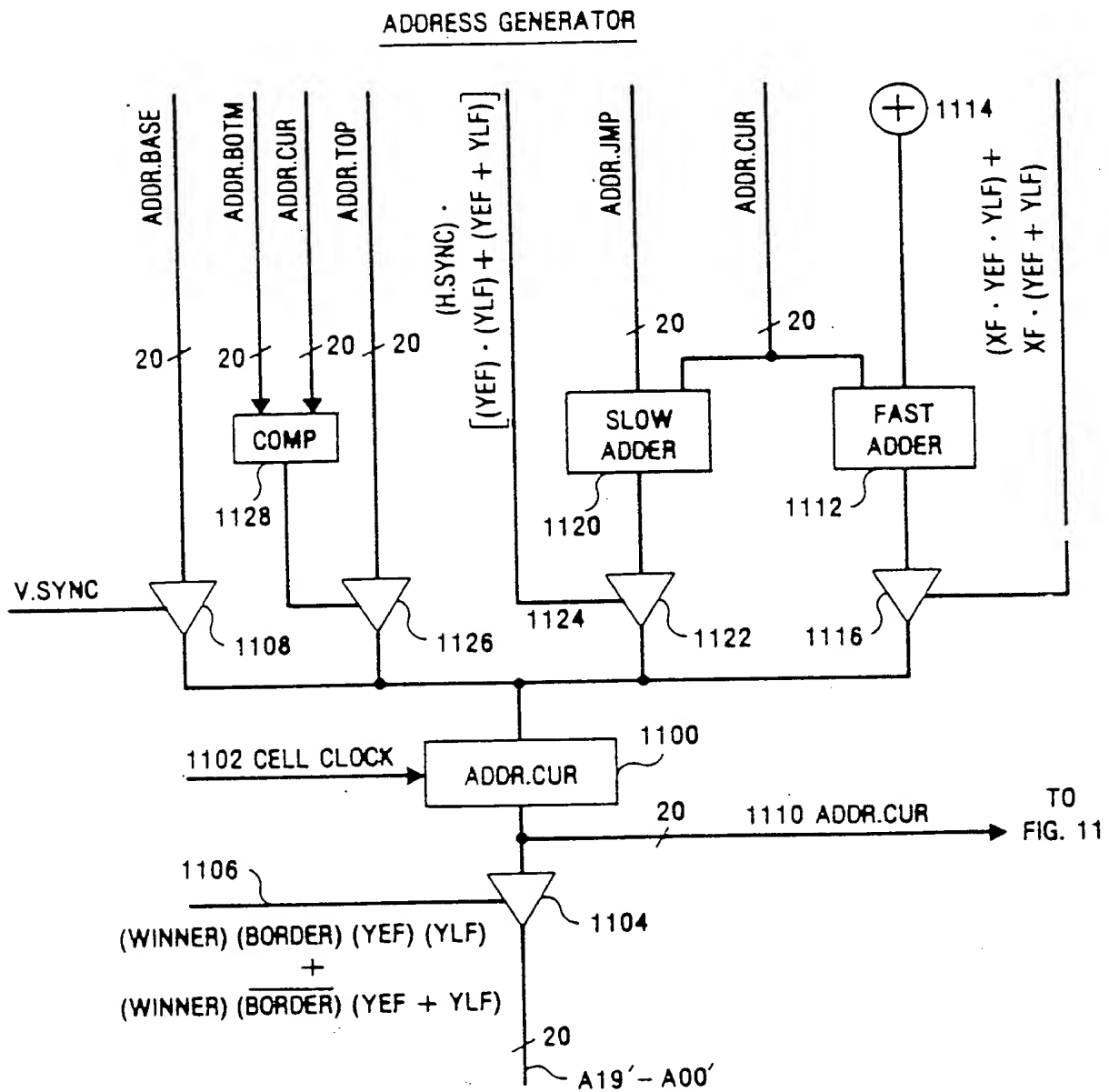


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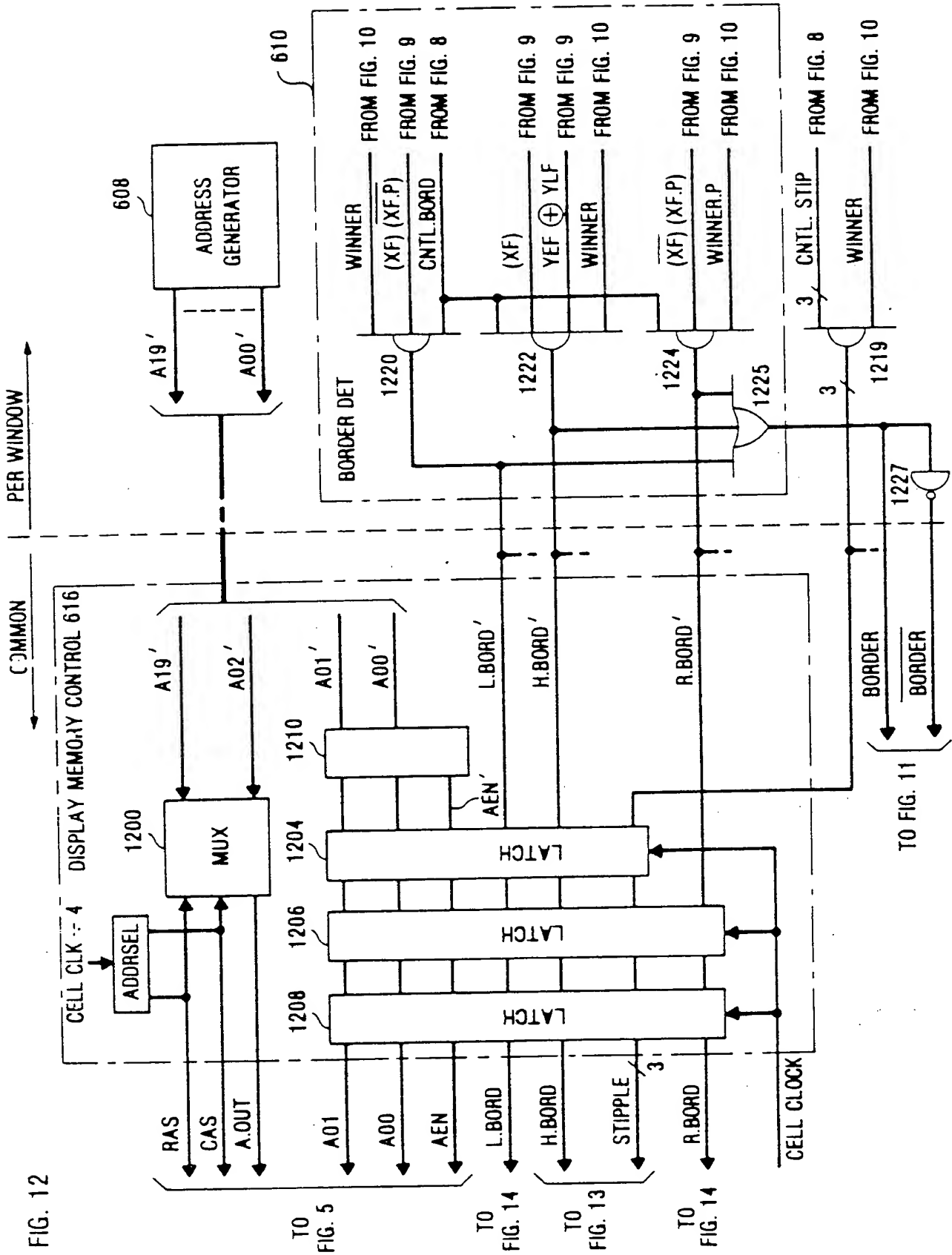


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FIG. 11



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FIG. 13

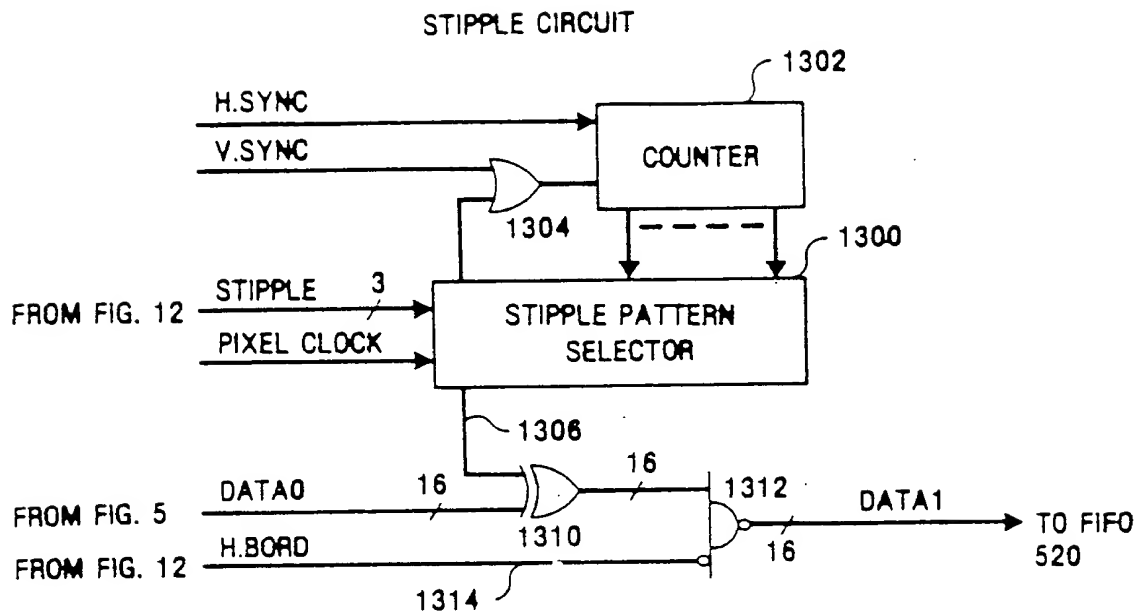
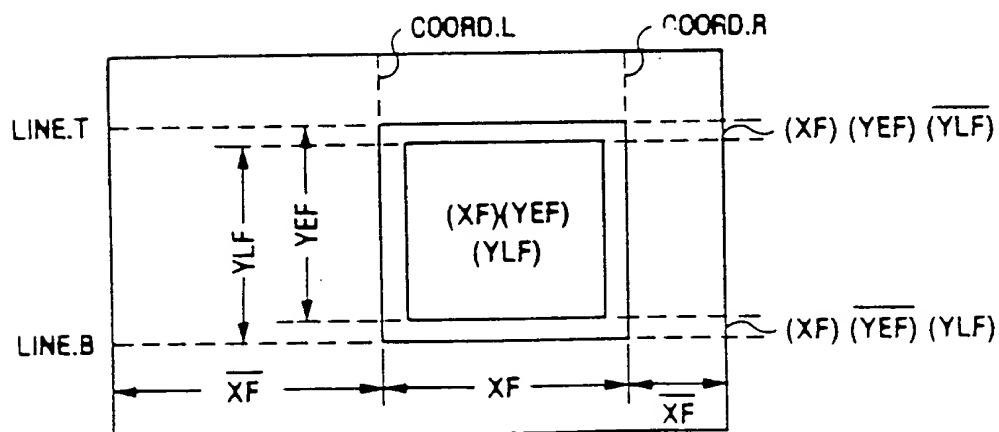


FIG. 15



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FIG. 14

